the pads (28) are the same. The wire connections (26) are completed after the die, as shown in Figure 1, is completely manufactured with discrete conductors already formed on the die (14). In the embodiment where device (22) is the end use device, the die will be first be KGD tested after forming metallurgical contacts between the stress tolerant solder ball array or flip-chip C4 array balls as illustrated in Figure 2. After KGD testing, the die (14) is removed from the test device (20) by melting the solder balls and separating the KGD from the device (20). Then, the die is installed in an end use device, as shown in Figure 3 by completion of a wire connections (26) between die (14) and end use device (22). In this embodiment, the stress tolerant solder ball connections to the test device provide an improved KGD test.---

Please replace the paragraph beginning at line 10 of page 18 with the following rewritten paragraph:

A3

---An exemplary die is shown the photographs of Figure 4 and 5 which can be alternatively used to test the die as a known good die either by a wire bond test described with respect Figure 3, or by a stress tolerant solder ball or flip-chip C4 array bond test as shown and described in Figure 2. Figure 5 is a photograph showing the actual ball and pad structure. Figure 6 shows the pads (12) and the balls (10) on the same planar surface of a wafer (32).---

Please replace the paragraph beginning at line 19 of page 19 with the following rewritten paragraph:

---In Figure 6 there is shown a segment of a wafer (32) having wire bond pads along the right and left hand edges. In the center of wafer (32) is a cluster of solder balls (10) which are laid out in a square grid surrounding a neutral point (18) of the wafer segment (32). The ball grid may be any size and its size depends only upon the number of connections required and the limitation of a number of connections imposed by spacing from the center (18). Shown on the wafer are a plurality of chips (34) which are interconnected into a multi chip module all on the surface of wafer segment (32). Testing of the wafer segment (32) is either by use of a stress tolerant solder ball array (10), or by use of wire bond pads (12) as described with respect to the embodiments above relating to single known good die production. Although wafer segment (32) contains the plurality of integrated circuits (34), it clearly is definable as an integrated circuit merely having sub-integrated circuits (34) all connected together on the surface of wafer (32).---

IN THE CLAIMS:

Please amend claim 1 as follows:

1. A known good integrated circuit device having optional solder ball array or wire bond connections:

solder ball array connections on an integrated circuit device surface;